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09/595,776	06/16/2000	Enric Musoll	P3810	1143

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PO BOX 187
AROMAS, CA 95004

EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	10

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/595,7[redacted]	MUSOLL ET AL.
	Examiner	Art Unit
	David J. Huisman	2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #5. Extension of Time as received on 3/4/2004, #6. RCE as received on 3/4/2004, #7. Amendment "B" as received on 3/4/2004, #8. Declaration as received on 3/9/2004, and #9. IDS as received on 3/9/2004.

Information Disclosure Statement

3. Applicant had filed an IDS on March 9, 2004, and did not provide hard copies for any of the disclosed reference because they were "filed in priority application 09/312,302." However, the IDS filed in 09/312,302 does not disclose any of the references on pages 4 and 5 of the IDS filed on March 9, 2004, for the instant application (except for the last reference on page 4). Therefore, these references are not being considered. In addition, the second and fourth references on page 3 of applicant's IDS filed on March 9, 2004 are not being considered because the examiner cannot quickly obtain a copy of these references and applicant has failed to provide a copy of these references in priority application 09/312,302. Rule 1.98(d) says that the IDS filed in the earlier application must comply with 1.98(a)-(c). However, the IDS in the earlier application fails to comply with 1.98(a)(2) in that a hard copy is not provided. Therefore, the IDS filed in the instant case fails to comply with 1.98(d).

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Amendment Format Comments

5. Applicant's amendment fails to comply with the revised 37 CFR 1.121, which is required as of July 30, 2003. More specifically, applicant has used "(Previously Amended)" as a status identifier for multiple claims. However, since this is an invalid identifier, the appropriate identifier would be "(Previously Presented)." In the future, the examiner will send out a notice of non-compliant amendment for failure to comply with the revised 37 CFR 1.121. Please see the attached flyer for more details.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627 (as applied in the previous Office Action), in view of McFarling et al., U.S. Patent No. 5,758,142 (as applied in the previous Office Action and herein referred to as McFarling).

8. Referring to claim 1, Parady has taught in a processor having multiple hardware streams supporting multiple data threads (Fig.3), and a data cache (Fig.1, component 56), a system for fetching instructions from individual ones of the multiple streams to a pipeline, comprising:
a) a fetch algorithm for selecting from which stream to fetch instructions. See the abstract. It should also be realized that when fetching instructions of a particular thread, the instructions will be fetched from the stream associated with those instructions, where the stream is the hardware that supports the instruction threads. For example, in Fig.3, each instruction buffer and each bus connecting the each instruction buffer to the dispatch unit is considered a stream since the buffers and wires are hardware in which the thread instructions reside and flow.
b) Parady has not taught a hit/miss predictor for forecasting whether instructions will hit or miss the data cache wherein the prediction by the hit/miss predictor is used by the fetch algorithm in determining from which stream to fetch. However, McFarling has taught a hit/miss predictor that is used to predict, for load instructions, whether a cache hit or miss will occur. And, if a cache miss is predicted to occur, then instructions independent of the load are scheduled ahead of the load-dependent instructions. See column 3, lines 7-18. A person of ordinary skill in the art would have recognized that this prediction scheme would be useful in a multiple-thread environment because a thread is a sequence of instructions that is independent from other threads (i.e. other sequences of instructions), as is known in the art. By implementing such a prediction scheme into the system of Parady, thread switches can occur sooner, thereby maximizing efficiency through execution of load-independent instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the thread-switching system of Parady to include a hit/miss predictor as taught by McFarling, in order to

switch threads before the load reaches the execution stage, thereby preventing a drop-off in throughput.

9. Referring to claim 2, Parady in view of McFarling has taught a system as described in claim 1. Furthermore, McFarling has taught that a hit prediction precipitates no change in the fetching process, i.e., the instructions dependent on the load will not be preempted by instructions independent of the load. See column 3, lines 7-18, and column 8, lines 28-49. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 1, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's system. In the combined Parady/McFarling system, if a hit prediction occurs, then instructions from the same thread will be fetched and executed.

10. Referring to claim 3, Parady in view of McFarling has taught a system as described in claim 1. Furthermore, McFarling has taught that a miss prediction results in switching fetching to a different stream, i.e., the instructions dependent on the load will be preempted by instructions independent of the load. See column 3, lines 7-18, and column 8, lines 28-49. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 1, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's system. In the combined Parady/McFarling system, if a miss prediction occurs, then instructions from a different thread will be fetched and executed.

11. Referring to claim 4, Parady in view of McFarling has taught a system as described in claim 1. Furthermore, McFarling has taught the hit/miss predictor determines a hit probability, and the probability is used by the fetch algorithm in determining from where to fetch next instructions. See column 8, line 50, to column 9, line 33. Note that a 2-bit saturating counter

(doesn't wrap-around) exists for each load instruction within the program. This counter is incremented if the load hits the cache and decremented if the load misses the cache. The most significant bit is then used to make the prediction (i.e. if the counter equals 10 or 11, a hit is predicted, otherwise a miss is predicted). Therefore, it can be seen that if the load always hits, the counter will saturate at a binary value of 11, which would always result in a hit prediction. This predictor determines a hit probability in that each possible value of the counter represents a different probability based on past experience. The higher the counter value, the higher the hit probability. For instance, a counter value of 11 signifies a load instruction that has hit the cache recently. Therefore, it will be predicted with a high hit probability. On the other hand, a counter value of 00 signifies a load instruction that has missed the cache recently. Therefore, it will be predicted with no hit probability, i.e., it will be predicted to miss. Generally, these extreme values (00 and 11) are considered to be strongly taken and strongly not-taken prediction values, respectively. Counter values of 01 and 10 can be considered not-taken and taken prediction values, respectively, but the probability is less that it will miss and less that it will hit, respectively. As a result, it can be seen that as the counter value increases, so does the hit probability, thereby indicating that a load with a counter value of 11 is much more likely to hit the cache than a load with a counter value of 00, according to past encounters. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 1, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's system. Note from above that the prediction directly results in what instruction are executed next. Therefore, in the combined Parady/McFarling system, higher probability hit predictions

will result in fetching from a different stream. Likewise, low probability hit predictions (miss predictions) will result in fetching from the same stream.

12. Referring to claim 5, Parady in view of McFarling has taught a system as described in claim 1. Furthermore, McFarling has taught that the forecast of the hit/miss predictor is also used by a dispatch algorithm in selecting instructions from the pipeline to dispatch to functional units. See column 3, lines 7-18, and column 8, lines 28-49, and note that when a miss occurs, the dispatcher will dispatch instructions based on the prediction. For example, if a hit prediction occurs, the dispatcher will continue dispatching instructions that may be dependent on the load. However, if a miss prediction occurs, the dispatcher will dispatch instructions that are independent of the load so that they do not have to wait for the result. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 1, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's system. In the combined Parady/McFarling system the dispatcher would work in the same fashion, i.e., if a hit prediction occurs, instructions from the same stream which may be dependent on the load can continue to be dispatched, while if a miss prediction occurs, then instructions from a different thread (independent of the load) will be dispatched.

13. Referring to claim 6, Parady has taught a processor having multiple hardware streams supporting multiple data threads (Fig.3), comprising:

a) a data cache. See Fig.1, component 56, and Fig.2, component 82.

b) a fetch algorithm for selecting from which stream to fetch instructions. See the abstract. It should also be realized that when fetching instructions of a particular thread, the instructions will be fetched from the stream associated with those instructions, where the stream is the hardware

that supports the instruction threads. For example, in Fig.3, each instruction buffer and each bus connecting the each instruction buffer to the dispatch unit is considered a stream since the buffers and wires are hardware in which the thread instructions reside and flow.

c) Parady has not taught a hit/miss predictor for predicting whether instructions will hit or miss the cache wherein a prediction by the hit/miss predictor is used by the fetch algorithm in determining from which stream to fetch. However, McFarling has taught a hit/miss predictor that is used to predict, for load instructions, whether a cache hit or miss will occur. And, if a cache miss is predicted to occur, then instructions independent of the load are scheduled ahead of the load-dependent instructions. See column 3, lines 7-18. A person of ordinary skill in the art would have recognized that this prediction scheme would be useful in a multiple thread environment because a thread is a sequence of instructions that is independent from other threads (i.e. other sequences of instructions), as is known in the art. By implementing such a prediction scheme into the system of Parady, thread switches can occur sooner, thereby maximizing efficiency through execution of load-independent instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the thread-switching system of Parady to include a hit/miss predictor as taught by McFarling, in order to switch threads before the load reaches the execution stage, thereby preventing a drop-off in throughput.

14. Referring to claim 7, Parady in view of McFarling has taught a processor as described in claim 6. Furthermore, McFarling has taught that a hit prediction precipitates no change in the fetching process, i.e., the instructions dependent on the load will not be preempted by instructions independent of the load. See column 3, lines 7-18, and column 8, lines 28-49. This

feature is part of McFarling's predictor, which as discussed in the rejection of claim 6, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's processor. In the combined Parady/McFarling system, if a hit prediction occurs, then instructions from the same thread will be fetched and executed.

15. Referring to claim 8, Parady in view of McFarling has taught a processor as described in claim 6. Furthermore, McFarling has taught that a miss prediction results in switching fetching to a different stream, i.e., the instructions dependent on the load will be preempted by instructions independent of the load. See column 3, lines 7-18, and column 8, lines 28-49. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 6, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's processor. In the combined Parady/McFarling system, if a miss prediction occurs, then instructions from a different thread will be fetched and executed.

16. Referring to claim 9, Parady in view of McFarling has taught a processor as described in claim 6. Furthermore, McFarling has taught the hit/miss predictor determines a hit probability, and the probability is used by the fetch algorithm in determining from where to fetch next instructions. See column 8, line 50, to column 9, line 33. Note that a 2-bit saturating counter (doesn't wrap-around) exists for each load instruction within the program. This counter is incremented if the load hits the cache and decremented if the load misses the cache. The most significant bit is then used to make the prediction (i.e. if the counter equals 10 or 11, a hit is predicted, otherwise a miss is predicted). Therefore, it can be seen that if the load always hits, the counter will saturate at a binary value of 11, which would always result in a hit prediction. This predictor determines a hit probability in that each possible value of the counter represents a

different probability based on past experience. The higher the counter value, the higher the hit probability. For instance, a counter value of 11 signifies a load instruction that has hit the cache recently. Therefore, it will be predicted with a high hit probability. On the other hand, a counter value of 00 signifies a load instruction that has missed the cache recently. Therefore, it will be predicted with no hit probability, i.e., it will be predicted to miss. Generally, these extreme values (00 and 11) are considered to be strongly taken and strongly not-taken prediction values, respectively. Counter values of 01 and 10 can be considered not-taken and taken prediction values, respectively, but the probability is less that it will miss and less that it will hit, respectively. As a result, it can be seen that as the counter value increases, so does the hit probability, thereby indicating that a load with a counter value of 11 is much more likely to hit the cache than a load with a counter value of 00, according to past encounters. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 6, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's processor. Note from above that the prediction directly results in what instruction are executed next. Therefore, in the combined Parady/McFarling system, higher probability hit predictions will result in fetching from a different stream. Likewise, low probability hit predictions (miss predictions) will result in fetching from the same stream.

17. Referring to claim 10, Parady in view of McFarling has taught a processor as described in claim 6. Furthermore, McFarling has taught that the forecast of the hit/miss predictor is also used by a dispatch algorithm in selecting instructions from the pipeline to dispatch to functional units. See column 3, lines 7-18, and column 8, lines 28-49, and note that when a miss occurs, the dispatcher will dispatch instructions based on the prediction. For example, if a hit prediction

occurs, the dispatcher will continue dispatching instructions that may be dependent on the load. However, if a miss prediction occurs, the dispatcher will dispatch instructions that are independent of the load so that they do not have to wait for the result. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 6, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's processor. In the combined Parady/McFarling system the dispatcher would work in the same fashion, i.e., if a hit prediction occurs, instructions from the same stream which may be dependent on the load can continue to be dispatched, while if a miss prediction occurs, then instructions from a different thread (independent of the load) will be dispatched.

18. Referring to claim 11, Parady has taught in a processor having multiple hardware streams supporting multiple data threads (Fig.3), and a data cache (see Fig.1, component 56, and Fig.2, component 82), a method for fetching instructions from individual ones of multiple streams as instruction sources to a pipeline (see the abstract). Parady has not taught making a hit/miss prediction by a predictor as to whether instructions previously fetched will hit or miss the data cache, and if the prediction is a miss, altering the source of the fetch. However, McFarling has taught a hit/miss predictor that is used to predict, for load instructions, whether a cache hit or miss will occur. And, if a cache miss is predicted to occur, then instructions independent of the load are scheduled ahead of the load-dependent instructions. See column 3, lines 7-18. A person of ordinary skill in the art would have recognized that this prediction scheme would be useful in a multiple-thread environment because a thread is a sequence of instructions that is independent from other threads (i.e. other sequences of instructions), as is known in the art. By implementing such a prediction scheme into the system of Parady, thread switches can occur sooner, thereby

maximizing efficiency through execution of load-independent instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the thread-switching system of Parady to include a hit/miss predictor as taught by McFarling, in order to switch threads before the load reaches the execution stage, thereby preventing a drop-off in throughput.

19. Referring to claim 12, Parady in view of McFarling has taught a method as described in claim 11. Furthermore, McFarling has taught the hit/miss predictor determines a hit probability, and the probability is used by the fetch algorithm in determining from where to fetch next instructions. See column 8, line 50, to column 9, line 33. Note that a 2-bit saturating counter (doesn't wrap-around) exists for each load instruction within the program. This counter is incremented if the load hits the cache and decremented if the load misses the cache. The most significant bit is then used to make the prediction (i.e. if the counter equals 10 or 11, a hit is predicted, otherwise a miss is predicted). Therefore, it can be seen that if the load always hits, the counter will saturate at a binary value of 11, which would always result in a hit prediction. This predictor determines a hit probability in that each possible value of the counter represents a different probability based on past experience. The higher the counter value, the higher the hit probability. For instance, a counter value of 11 signifies a load instruction that has hit the cache recently. Therefore, it will be predicted with a high hit probability. On the other hand, a counter value of 00 signifies a load instruction that has missed the cache recently. Therefore, it will be predicted with no hit probability, i.e., it will be predicted to miss. Generally, these extreme values (00 and 11) are considered to be strongly taken and strongly not-taken prediction values, respectively. Counter values of 01 and 10 can be considered not-taken and taken prediction

values, respectively, but the probability is less that it will miss and less that it will hit, respectively. As a result, it can be seen that as the counter value increases, so does the hit probability, thereby indicating that a load with a counter value of 11 is much more likely to hit the cache than a load with a counter value of 00, according to past encounters. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 11, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's method. Note from above that the prediction directly results in what instruction are executed next. Therefore, in the combined Parady/McFarling system, higher probability hit predictions will result in fetching from a different stream. Likewise, low probability hit predictions (miss predictions) will result in fetching from the same stream.

20. Referring to claim 13, Parady in view of McFarling has taught a method as described in claim 11. Furthermore, McFarling has taught that the forecast of the hit/miss predictor is also used by a dispatch algorithm in selecting instructions from the pipeline to dispatch to functional units. See column 3, lines 7-18, and column 8, lines 28-49, and note that when a miss occurs, the dispatcher will dispatch instructions based on the prediction. For example, if a hit prediction occurs, the dispatcher will continue dispatching instructions that may be dependent on the load. However, if a miss prediction occurs, the dispatcher will dispatch instructions that are independent of the load so that they do not have to wait for the result. This feature is part of McFarling's predictor, which as discussed in the rejection of claim 1, would have been obvious to one of ordinary skill in the art at the time of the invention to implement in Parady's method. In the combined Parady/McFarling system the dispatcher would work in the same fashion, i.e., if a hit prediction occurs, instructions from the same stream which may be dependent on the load

can continue to be dispatched, while if a miss prediction occurs, then instructions from a different thread (independent of the load) will be dispatched.

Response to Arguments

21. Applicant's arguments filed on March 9, 2004, have been fully considered. In general, Applicant argues the novelty/rejection of claims 1, 6, and 11, in that the examiner should be interpreting the word "stream" in the claims based on the definition of "stream" provided in Applicant's specification. The examiner wants to make the applicant aware of the following:

"Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art." *In re Self*, 213 USPQ 1,5 (CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978).

Consequently, the examiner asserts that the definition of "stream" provided by the examiner in the previous Office Action was sufficient enough to read on "stream" as it appeared in the claims. The examiner would not have considered a "stream" as being "a small river" as applicant suggests because this definition is non-analogous to the art of computer architecture. It should be realized that even if the examiner uses the "stream" definition provided by applicant, Parady still anticipates the claim. More specifically, applicant has defined a stream as being hardware for supporting and processing an instruction thread (from the specification) and similarly, streams are the hardware resources which support flows of data defined as threads (from page 5 of the arguments). Looking at Fig.3 of Parady, it is clear that Parady's system

processes multiple threads (it processes threads 0, 1, 2, and 3). The instructions associated with thread 0 are stored in a first buffer 102. The instructions associated with thread 1 are stored in a second buffer 104, and so on. These instructions are then propagated to the dispatch unit where they will be dispatched to the execution units. Clearly, if Parady's system supports and processes multiple threads, then streams, i.e., the hardware to support and process instruction threads, must inherently exist. From Fig.3, all of the hardware shown is used to support and process an instruction thread, from the instruction buffers which hold thread instructions to the buses that allow the thread data to flow throughout the system (for example, from the instruction buffers to the dispatch unit). As a result, the examiner asserts that Parady still reads on applicant's claims even when applicant's definition of "stream" is used.

22. In the remarks, Applicant argues the novelty/rejection of claims 1, 6, and 11 on page 6 of the remarks, in substance that:

> "Applicant strongly maintains that the examiner's combination of the teachings of Parady and McFarling remains improper, as McFarling teaches nothing whatsoever to do with a multistream processor, and the invention of McFarling, therefore, does not have the capability of being obviously practiced in the invention of Parady."

23. These arguments are not found persuasive for the following reasons:

a) As previously stated, the examiner used McFarling to show a teaching of a hit/miss predictor that is used to predict, for load instructions, whether a cache hit or miss will occur, and, if a cache miss is predicted to occur, then instructions independent of the load are scheduled ahead of the load-dependent instructions. See column 3, lines 7-18, of McFarling. This is relevant to Parady because a given thread is independent of other threads. Consequently, much like scheduling load-independent instructions ahead of load-dependent instructions that are predicted

to miss the cache (in McFarling), one of ordinary skill in the art would have recognized that thread-independent instructions (i.e., instructions from a second thread) could be scheduled ahead of instructions that are dependent on a load in the first thread that is predicted to miss the cache. More specifically, in Parady in view of McFarling, if instructions were being fetched from a first thread (i.e., from thread 0's instruction buffer) and a load instruction within thread 0's is predicted to miss the cache, then according to McFarling, instructions from a second thread would be dispatched, say from thread 1's instruction buffer, in order to prevent stalling. This is because thread 1's instructions would be independent of thread 0 and they would not be dependent on a load within thread 0 that would possibly miss the cache. By implementing such a prediction scheme into the system of Parady, thread switches would occur sooner, thereby maximizing efficiency through execution of load-independent instructions. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the thread-switching system of Parady to include a hit/miss predictor as taught by McFarling, in order to switch threads before the load reaches the execution stage, thereby preventing a drop-off in throughput.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
April 28, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

REVISED AMENDMENT PRACTICE: 37 CFR 1.121 CHANGED COMPLIANCE IS MANDATORY - Effective Date: July 30, 2003

All amendments filed on or after the effective date noted above must comply with revised 37 CFR 1.121. See Final Rule: **Changes To Implement Electronic Maintenance of Official Patent Application Records** (68 *Fed. Reg.* 38611 (June 30, 2003), posted on the Office's website at: http://www.uspto.gov/web/patents/ifw/ with related information. The amendment practice set forth in revised 37 CFR 1.121, and described below, replaces the voluntary revised amendment format available to applicants since February 2003. **NOTE: STRICT COMPLIANCE WITH THE REVISED 37 CFR 1.121 IS REQUIRED AS OF THE EFFECTIVE DATE (July 30, 2003).** The Office will notify applicants of amendments that are not accepted because they do not comply with revised 37 CFR 1.121 via a Notice of Non-Compliant Amendment. See MPEP 714.03 (Rev. 1, Feb. 2003). The non-compliant section(s) will have to be corrected and the entire corrected section(s) resubmitted within a set period.

Bold underlined italic font has been used below to highlight the major differences between the revised 37 CFR 1.121 and the voluntary revised amendment format that applicants could use since February, 2003.
Note: The amendment practice for **reissues** and **reexamination proceedings**, except for drawings, has not changed.

REVISED AMENDMENT PRACTICE

I. Begin each section of an amendment document on a separate sheet:
Each section of an amendment document (*e.g.*, Specification Amendments, Claim Amendments, Drawing Amendments, and Remarks) must begin on a separate sheet. Starting each separate section on a new page will facilitate the process of separately indexing and scanning each section of an amendment document for placement in an image file wrapper.

II. Two versions of amended part(s) no longer required:
37 CFR 1.121 has been revised to no longer require two versions (a clean version and a marked up version) of each replacement paragraph or section, or amended claim. Note, however, the requirements for a clean version and a marked up version for substitute specifications under 37 CFR 1.125 have been retained.

A) Amendments to the claims:
Each amendment document that includes a change to an existing claim, cancellation of a claim or submission of a new claim, **must include a complete listing** of all claims in the application. After each claim number in the listing, the status must be indicated in a parenthetical expression, and **the text of each pending claim** (with markings to show current changes) must be presented. The claims in the listing will replace all prior claims in the application.

(1) The current status of all of the claims in the application, including any previously canceled, not entered or withdrawn claims, must be given in a parenthetical expression following the claim number using only one of the following seven status identifiers: (original), (currently amended), (canceled), (withdrawn), (new), ***(previously presented) and (not entered).*** The text of all pending claims, ***including withdrawn claims,*** must be submitted each time any claim is amended. Canceled ***and not entered*** claims must be indicated by only the claim number and status, without presenting the text of the claims.

(2) The text of all claims being currently amended must be presented in the claim listing with markings to indicate the changes that have been made relative to the immediate prior version. The changes in any amended claim must be shown by underlining (for added matter) or strikethrough (for deleted matter) with 2 exceptions: (1) for ***deletion of five characters or fewer, double brackets may be used (e.g., [[eroor]]); and (2) if strikethrough cannot be easily perceived (e.g., deletion of the number "4" or certain punctuation marks), double brackets must be used (e.g., [[4]]). As an alternative to using double brackets, however, extra portions of text may be included before and after text being deleted, all in strikethrough, followed by including and underlining the extra text with the desired change*** *(e.g., ~~number 4 as~~ number 14 as).* An accompanying clean version is not required and should not be presented. Only claims of the status "currently amended," and "withdrawn" that are being amended, may include markings.

(3) The text of pending claims not being currently amended, ***including withdrawn claims,*** must be presented in the claim listing in clean version, *i.e.*, without any markings. Any claim text presented in clean version will constitute an assertion that it has not been changed relative to the immediate prior version except to omit markings that may have been present in the immediate prior version of the claims.

(4) A claim being canceled must be listed in the claim listing with the status identifier "canceled"; the text of the claim must not be presented. Providing an instruction to cancel is optional.
(5) Any claims added by amendment must be presented in the claim listing with the status identifier "(new)"; the text of the claim must not be underlined.
(6) All of the claims in the claim listing must be presented in ascending numerical order. Consecutive canceled, or not entered, claims may be aggregated into one statement (*e.g.*, Claims 1 – 5 (canceled)).

Example of listing of claims (use of the word "claim" before the claim number is optional):

Claims 1-5 (canceled)

Claim 6 (previously presented): A bucket with a handle.

Claim 7 (withdrawn): A handle comprising an elongated wire.

Claim 8 (withdrawn): The handle of claim 7 further comprising a plastic grip.

Claim 9 (currently amended): A bucket with a ~~green~~ blue handle.

Claim 10 (original): The bucket of claim 9 wherein the handle is made of wood.

Claim 11 (canceled)

Claim 12 (not entered)

Claim 13 (new): A bucket with plastic sides and bottom.

B) Amendments to the specification:
Amendments to the specification, including the abstract, must be made by presenting a replacement paragraph or section or abstract marked up to show changes made relative to the immediate prior version. An accompanying clean version is not required and should not be presented. Newly added paragraphs or sections, including a new abstract (instead of a replacement abstract), must not be underlined. A replacement or new abstract must be submitted on a separate sheet, 37 CFR 1.72. If a substitute specification is being submitted to incorporate extensive amendments, both a clean version (which will be entered) and a marked up version must be submitted as per 37 CFR 1.125.

The changes in any replacement paragraph or section, or substitute specification must be shown by underlining (for added matter) or strikethrough (for deleted matter) with 2 exceptions: (1) for ***deletion of five characters or fewer, double brackets may be used (e.g., [[eroor]]; and (2) if strikethrough cannot be easily perceived (e.g., deletion of the number "4" or certain punctuation marks), double brackets must be used (e.g., [[4]]). As an alternative to using double brackets, however, extra portions of text may be included before and after text being deleted, all in strikethrough, followed by including and underlining the extra text with the desired change*** *(e.g., ~~number 4 as~~ number 14 as)*

C) Amendments to drawing figures:
Drawing changes must be made by presenting replacement figures which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments, or remarks, section of the amendment, ***and may be accompanied by a marked-up copy of one or more of the figures being amended, with annotations.*** Any replacement drawing sheet must ***be identified in the top margin as "Replacement Sheet"*** and include all of the figures appearing on the immediate prior version of the sheet, even though only one figure may be amended. ***Any marked-up (annotated) copy showing changes must be labeled "Annotated Marked-up Drawings" and accompany the replacement sheet in the amendment (e.g., as an appendix).*** The figure or figure number of the amended drawing(s) must **not** be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Questions regarding the submission of amendments pursuant to the revised practice set forth in this flyer should be directed to: Elizabeth Dougherty or Gena Jones, Legal Advisors, or Joe Narcavage, Senior Special Projects Examiner, Office of Patent Legal Administration, by e-mail to patentpractice@uspto.gov or by phone at (703) 305-1616.